AMENDMENTS TO THE CLAIMS

Please cancel claim 6 without prejudice or disclaimer of its underlying subject matter.

1-24. (Canceled).

25. (Currently amended) A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a general driver horizontal shift register circuit and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a remainder driver horizontal shift register circuit and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits, and

said quantity of said general driver circuit output terminals being different than said quantity of said remainder driver circuit output terminals.

26. (Currently amended) A display according to claim 25, wherein ~~each~~ one driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. (Previously presented) A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

28. (Previously presented) A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. (Previously presented) A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

30. (Canceled).

31. (Previously presented) A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

32-36. (Canceled).

37. (Previously presented) A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

38-42. (Canceled).

43. (Previously presented) A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. (Previously presented) A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. (Previously presented) A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

46. (Currently amended A display according to claim 25, wherein said plurality of driver circuits includes more than one said general driver circuit.

47. (Currently amended) A display according to claim 46, wherein said each said at least one general driver circuit has an equal number of general driver circuit output terminals.

48. (Previously presented) A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

49. (Previously presented) A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, each of said plurality of driver circuits having a plurality of driver circuit output terminals,

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines,

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits, and

the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

50. (Previously presented) A display according to claim 49, further comprising:

a plurality of time-divisional switches, said plurality of time-divisional switches receiving said signal potential from said driver circuit output terminal and time-divisionally sending said received signal potential said signal line.

51. (Previously presented) A display according to claim 50, wherein the quantity of said time-divisional switches is equal to 3.

52. (Previously presented) A display according to claim 49, wherein said quantity of said signal lines is different than said quantity of said driver circuit output terminals.

53. (Previously presented) A display according to claim 49, wherein said quantity of said driver circuit output terminals is set to a power of 2.

54. (Previously presented) A display according to claim 49, wherein said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrate on which said display portion is formed.

55. (Previously presented) A display according to claim 49, further comprising:

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

56. (Previously presented) A display according to claim 49, wherein a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

57. (Previously presented) A display according to claim 49, wherein a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

58. (Previously presented) A display according to claim 57, wherein a leading time and a trailing time of each of said plurality of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches.

59. (Previously presented) A display according to claim 49, wherein a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period - the period of time selected by the time-divisional switches x 3) / 3.

60. (Previously presented) A display according to claim 59, wherein said plurality of driver circuits have a function to stop the operation of an output circuit of said plurality of driver circuits for said blanking period.

61. (Previously presented) A display according to claim 49, wherein said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) by diving to said time-divisional switches.

62. (Previously presented) A display according to claim 49, wherein within a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

63. (Previously presented) A display according to claim 49, wherein within a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

64. (Previously presented) A display according to claim 49, wherein time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

65. (Previously presented) A display according to claim 49, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

66. (Previously presented) A display according to claim 49, wherein said driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

Please add the following new claims.

67. (New) A display according to claim 49, wherein said each of said plurality of driver circuits has a horizontal shift register circuit.

68. (New) A display according to claim 67, wherein one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits.

69. (New) A display according to claim 67, wherein said horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses.

70. (New) A display according to claim 67, wherein said horizontal shift register circuit has sampling switches, a level shifter, a data latch circuit, and a digital/analog converting circuit.

71. (New) A display according to claim 25, wherein one general driver horizontal shift register circuit of said plurality of driver circuits is separate and distinct from another general driver horizontal shift register circuit of said plurality of driver circuits.

72. (New) A display according to claim 25, wherein said general driver horizontal shift register circuit performs a horizontal scan by sequentially generating horizontal scanning pulses.

73. (New) A display according to claim 25, wherein said each said at least one general driver circuit has general driver sampling switches, a general driver level shifter, a general driver data latch circuit, and a general driver digital/analog converting circuit.

74. (New) A display according to claim 73, wherein sampling switches in said general driver sampling switches sequentially sample input digital image data in response to horizontal scanning pulses from said general driver horizontal shift register circuit.

75. (New) A display according to claim 73, wherein said general driver level shifter boosts digital data sampled by said general driver sampling switches to digital data of a liquid crystal driving voltage.

76. (New) A display according to claim 73, wherein said general driver data latch circuit is a memory to accumulate digital data boosted by said general driver level shifter by an amount of one horizontal period.

77. (New) A display according to claim 73, wherein said general driver digital/analog converting circuit converts digital data of one horizontal period which is outputted from said general driver data latch circuit into an analog signal and outputs said analog signal.

78. (New) A display according to claim 73, wherein said remainder driver circuit has remainder driver sampling switches, a remainder driver level shifter, a remainder driver data latch circuit, and a remainder driver digital/analog converting circuit.